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09/987,607	11/15/2001	Hongyong Zhang	740756-2395	7367
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ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			EXAMINER CHEN, JACK S J	
			ART UNIT 2813	PAPER NUMBER
			MAIL DATE 10/31/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

09/987,607

Applicant(s)

ZHANG, HONGYONG

Examiner

Jack Chen

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 7-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-5, 7-18 and 20-23 is/are allowed.
- 6) ☒ Claim(s) 1, 19, 24-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 24-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Re claims 24 and 27, the phrase "the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first interlayer insulating film and the second interlayer insulating film" is not described in the original specification. The remaining claims are rejected for depending from the above rejected claims. For the purpose of patentability, these claims will be interpreted as best understood.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Katami, JP/62-274729.
5. Katami discloses a method for forming a semiconductor device, which comprises forming an interlayer insulator comprising at least an upper layer comprising silicon nitride 106 and a lower layer comprising silicon oxide 105, each comprising different dry etching characteristics (see figs. 1A-1G); etching the upper layer 106 of the interlayer insulator using a first mask 107, wherein the lower layer 105 of the interlayer insulator is used as an etching stopper (see figs. 1A-1G); forming a second mask 107 to cover a portion of the lower layer of the interlayer insulator, which is exposed by the etching step (see figs. 1A-1G; specifically noting the overlap of the photoresist 107, in figs. 1e and 1F, due to the isotropic etchant); and selectively etching the lower layer of the interlayer insulator using the second mask 107 to form a contact hole (see figs. 1a-1g).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
7. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katami, JP/62-274729.
8. Katami disclosed above; however, Katami is silent to the claimed thickness (Re claim 24) of the second interlayer insulating film.

With respect to claim 24, the claimed thickness ranges of the second interlayer insulating film, absent evidence of disclosure of criticality for the range giving unexpected results are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller* 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious. *See also In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable thickness for the second interlayer insulating film in the method of Katami in order to provide proper isolation and/or as the matter of design choice.

Further in this regard, the specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first and second interlayer insulating film) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen arrangements are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

9. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang, US/5,635,423 in view of Roach, US/5,063,378.

Huang et al. teaches forming a first interlayer insulating film (53 or 63) on a surface (See columns 6-7 lines 47-44 and Figures 5(a)-5(c) and 6(a)-6(c)); forming a second interlayer insulating film (54 and 64) on the first interlayer insulating film (53 or 63), wherein the second interlayer insulating film has a different etching characteristic from the first interlayer insulating film (See columns 6-7 lines 47-44 and Figures 5(a)-5(c) and 6(a)-6(c)); forming an opening in the second interlayer insulating film by first etching to expose a surface of the first interlayer insulating film wherein the first interlayer insulating film functions as an etching stopper during the first etching (See columns 6-7 lines 47-44 and Figures 5(a)-5(c) and 6(a)-6(c)); and forming an opening in the first interlayer insulating film by second etching the exposed surface of the first interlayer insulating film (See columns 6-7 lines 47-44 and Figures 5(a)-5(c) and 6(a)-6(c)).

Huang et al. fails to explicitly teach wherein the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first and second interlayer insulating film.

With respect to claim 24, the claimed thickness ranges of the second interlayer insulating film, absent evidence of disclosure of criticality for the range giving unexpected results are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller* 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious. *See also In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson*

*56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable thickness for the second interlayer insulating film in the method of Huang et al. in order to provide proper isolation and/or as the matter of design choice.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first and second interlayer insulating film) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen arrangements are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

Additionally, the Examiner has not given patentable weight to the preamble limitation of "comprising at least one thin film transistor" because "[A] claim preamble has the import that the claim as a whole suggests for it". *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995) "If the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give, life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim." *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999). As the body of the claim makes no reference, nor allusion, to at least one thin film transistor (i.e. - the preamble does not recite limitations of the claim), and

since the above referenced preamble limitation does not give life or meaning to the claim, it is deemed to be of no patentable weight. See MPEP § 2111.02.

With respect to claim 26, Huang et al. fails to explicitly teach wherein the semiconductor device is a liquid crystal display device.

However, Roach, in columns 5-6 lines 60-20 and Figures 1-3, teaches etching contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode. Furthermore, Roach teaches that one would do this to provide metallization contacts to the TFT.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Huang et al. by incorporating the etching of contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode, as taught by Roach (i.e., for LCD device), to provide metallization contacts to the TFT.

10. Claims 19 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katami, JP/62-274,729 in view of Roach, US/5,063,378.

Katami disclosed above; however, Katami fails to explicitly teach wherein the semiconductor device is a liquid crystal display device (Re claims 19 and 26).

However, Roach, in columns 5-6 lines 60-20 and Figures 1-3, teaches etching contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode. Furthermore, Roach teaches that one would do this to provide metallization contacts to the TFT.



Therefore, it would have been obvious to one of ordinary skill in the art to modify Katami by incorporating the etching of contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode, as taught by Roach (i.e., for LCD device), to provide metallization contacts to the TFT.

Re claim 27, Katami, in Figures 1A-1 G, the Abstract and the Constitution, teaches: forming a semiconductor island on an insulating surface; forming a gate insulating film comprising silicon dioxide on the semiconductor island; forming a gate electrode over the semiconductor island with the gate insulating film interposed therebetween; forming a first insulating film (105) comprising silicon dioxide over the gate insulating film and the gate electrode; forming a second insulating film (106) comprising silicon nitride on the first silicon dioxide insulating film; first etching the second insulating film to form an opening wherein said silicon dioxide film functions as an etching stopper; second etching a portion of the first insulating film in accordance with the opening of the second insulating film, thereby, exposing a surface of the semiconductor layer.

Katami fails to explicitly teach the gate insulating film being etched and wherein the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first and second interlayer insulating film.

With respect to claim 27, the claimed thickness ranges of the second interlayer insulating film, absent evidence of disclosure of criticality for the range giving unexpected results are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller 105 USPQ233, 255 (CCPA 1955)*, the selection of

reaction parameters such as temperature and concentration would have been obvious. *See also In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable thickness for the second interlayer insulating film in the method of Katami in order to provide proper isolation and/or as the matter of design choice.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first and second interlayer insulating film) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen arrangements are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990). Since the element of criticality has not been met, the limitation concerning the second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of the first and second interlayer insulating film, is given no patentable weight.

Furthermore, Roach, in Figure 3, shows contact vias etched through an extended gate oxide layer of a thin film transistor. Finally, Roach teaches etching through the extended gate oxide layer to create an uninhibited contact to the source/drain region.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Katami to incorporate etching through an extended gate oxide layer of a thin film transistor, as taught by Roach, to create an uninhibited contact to the source/drain region.

With respect to claim 28, Katami fails to explicitly teach wherein the semiconductor device is a liquid crystal display device.

However, Roach, in columns 5-6 lines 60-20 and Figures 1-3, teaches etching contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode. Furthermore, Roach teaches that one would do this to provide metallization contacts to the TFT.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Katami by incorporating the etching of contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode, as taught by Roach (i.e., for LCD device), to provide metallization contacts to the TFT.

#### ***Reasons For Allowance***

11. Claims 2-5, 7-18 and 20-23 are allowable over the prior art of record.
12. The following is an examiner's statement of reasons for allowance: claims 2-5, 7-18 and 20-23 are allowed for reasons deemed to be of record.

#### ***Response to Arguments***

13. Applicant's arguments filed 6/17/04 have been fully considered but they are not persuasive.

14. Applicant argues that the Katami does not teach forming a second mask to cover a portion of the lower layer of the interlayer insulator, which is exposed by the etching step. Examiner respectfully disagrees because the claimed feature(s) is shown in fig. 1e. For example, second mask 107 covers at least a portion of the lower layer 105 (fig. 1e) of the interlayer insulator, which is exposed by the etching step (see figs. 1A-1G; specifically noting the overlap of the photoresist 107, in figs. 1e and 1F, due to the isotropic etchant).

***Conclusion***

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (8:00am-4:30pm).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Jack Chen  
Primary Examiner  
Art Unit 2813

October 27, 2007